REMARKS

Claims 1-15 are pending in the application and the same are rejected. By this Amendment, claims 1, 6, and 9 are amended. Accordingly, claims 1-15 remain in the application and are presented for review and further consideration by the Examiner.

The Examiner has rejected claims 1-4 and 6-11 under 35 U.S.C. §102(b) as being anticipated by Hamasaki, U.S. Patent No. 5,335,008. (Examiner's Action, page 2, ¶ 2).

Applicant respectfully disagrees.

Hamasaki discloses a CCD image sensing device having floating diffusion amplifiers 5 and a vertical signal line 9. The floating diffusion amplifiers 5 includes a storage (ST) section 1, an output gate (OG) switch 2, a reset MOS-FET 3, and an amplifying MOS-FET 4. When light becomes incident on each pixel of a CCD, a signal charge corresponding to the incident light is stored in the storage (ST) section 1. The storage section 1 and the output gate (OG) switch 2 constitute a CCD of one bit.

A horizontal line for each floating diffusion amplifiers 5 is selected by applying an output gate pulse Φ_{OG} to the gate electrode of the output gate switch 2, a reset gate pulse Φ_{RG} to the gate electrode of the reset MOS-FET 3, and a reset drain pulse Φ_{RD} to the drain electrode of the reset MOS-FET 3. When the horizontal line is selected, signal charges of full pixels of the horizontal line are amplified by the amplifying MOS-FET 4 and then output to the vertical signal line 9 as signal, V_{OUT}.

By convention, V_{OUT} is the symbol for a voltage signal. Thus, Hamasaki is indicating that the output onto vertical signal line 9 is a voltage and not a charge signal. The fact that the signal V_{OUT} is a voltage signal, rather than a charge signal, is reinforced in several ways. It is well known in the art that floating diffusion amplifiers convert charge to voltage and output a voltage signal. V_{OUT} is the output of floating diffusion amplifier 5, and therefore must be a voltage signal. Additionally, noise in V_{OUT} is filtered out using a noise eliminating capacitor C_0. It

is well known in the art that a capacitor can be used to filter noise from a voltage signal, but not a charge signal. Since Hanasaki is using a capacitor to filter noise in the V_{OUT} signal, the V_{OUT} signal must be a voltage signal and not a charge signal.

Since V_{OUT} is a voltage signal, change-over switch 14 is a voltage switch and not a charge switch or a charge demultiplexor. Therefore, Hamasaki does not disclose a charge demultiplexor.

In contrast, Applicant's independent claims 1, 6, and 9 include wording that a charge demultiplexor is configured to receive an output charge of a charge shift register and to selectively distribute the output charge to each of the at least two charge sensing nodes. Hamasaki does not disclose any structure that is configured to receive an output charge of a charge shift register and to selectively distribute the output charge to each of the at least two charge sensing nodes.

In addition, since the signal received from the change-over switch 14 is a voltage signal and not a charge signal, the sample and hold capacitors C1 and C2 of Hamasaki cannot be charge sensing nodes for accumulating charge. This is consistent with the well known function of sample and hold capacitors. Sample and hold capacitors sample and hold voltage, not charge. Therefore, Hamasaki does not disclose charge sensing nodes that accumulate charge, readable as a voltage.

In contrast, Applicant's independent claims 1, 6, and 9 include wording that at least two charge sensing nodes accumulate charge, readable as a voltage. Hamasaki does not disclose any structure that accumulates charge, readable as a voltage.

Furthermore, the Examiner improperly refers to the vertical line 9 as a vertical register. Vertical line 9 is not a register. Nothing in Hamasaki suggests that vertical line 9 is anything other than a signal output line for the outputs of the MOS-FETs 4. Nor does Hamasaki disclose any other structure that may properly

be considered a charge shift register configured to sequentially receive the charge from each cell.

In order to more clearly distinguish the vertical line 9 of Hamasaki from the present invention, Applicant has amended independent claims 1, 6, and 9 to further define the charge shift register as having a plurality of charge containers for storing charge. The vertical line 9 of Hamasaki is not disclosed as having a plurality of charge containers for storing charge.

In contrast, Applicant's independent claims 1, 6, and 9, as amended, include wording that a charge shift register has a plurality of charge containers for storing charge and is configured to sequentially shift charges between the charge containers. Since Hamasaki does not disclose a charge shift register having a plurality of charge containers.

The Examiner has rejected claims 5, 12, and 13-15 under 35 U.S.C. §103(a) as being unpatentable over Hamasaki, U.S. Patent No. 5,335,008, in view of Sawanobori, U.S. Patent No. 5,956,086. (Examiner's Action, page 7, ¶ 4).

Applicant respectfully disagrees.

In view of Applicant's arguments and amendments with respect to independent claims 1, 6, and 9 being allowable, Applicant respectfully submits that the remaining dependent claims are also allowable because they contain all of the limitations of their respective independent claims and further add structural and functional limitations.

The foregoing amendments and arguments are believed to be a complete response to the most recent Examiner's Action.

No new matter has been added.

It is respectfully submitted that there is no claim, teaching, motivation, or suggestion in any of the prior art cited, alone or in combination, to produce what Applicant claims.

It is further submitted that the application, as amended, defines patentable subject matter and that the claims are in a condition for allowance. Such allowance at an early date is respectfully requested.

Should any issues remain which would preclude the prompt disposition of this case, it is requested that the Examiner contact the undersigned practitioner by telephone.

Respectfully submitted,
Oscar R. Herrera E.

By 
Mark G. Pannell
Reg. No. 40,761

Date July 20, 2005
(719) 260-7900